SAR SIGNAL PROCESSING SYSTEMDESIGN AND FLEXIBLE HIGH-PERFORMANCE ANALYSIS

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Abstract:- ***The core of a radar network is the signal handling subsystem, the presentation and structure style of which may have a significant influence on the execution of the whole framework. Therefore, one of the biggest problems these days is how to recognize a superior adaptive all inclusive constant SAR signal handling system. With the new TI multi-center DSP TMS320C6678 based on the VPX 3U standard, the paper proposes the plan design and implementation of an elite continuous SAR signal preparing system. It illustrates the solid ability to measure, solidity, quick remaking and great versatility for a range of imaging calculations. The adaptability and elite could be satisfactorily illustrated by the fruitful implementation instances of the multi-mode, multi-polarization, multi-goals space-borne and airborne constant SAR imaging frameworks. In comparison, our test result reveals that a SAR RD measurement requires 21.55s for a 4GB (16K ?? 32K complicated focuses) image with 0.2m*0.2m targets, achieving continuous execution.***
Keywords-Processing of real-time signals; TMS320C6678; Universal; SAR imagery; High performance;

I. INTRODUCTION

Synthetic Aperture Radar (SAR) is an efficient high-resolution microwave sensor device developed in the 1950s by Wiley. The manner in which the human-made vision mechanism is built has been revolutionized [1]. SAR has numerous benefits, in comparison to other imaging techniques, such as outstanding penetrability, good anti-jamming capabilities and all-time suitability, etc. [8] SAR is a high-performance real-time processing system [8].

A computing platform that can complete the requisite imaging task in a specified short time. SAR technology has been widely adopted after years of growth, and it plays an increasingly crucial role in numerous fields, including geological mapping, marine exploration, military surveillance and other areas.

The huge volume of data and the real-time high-resolution radar imaging computing challenge placed higher demands on the real-time signal processing device and accelerated its growth. The introduction of several high-performance processors such as FPGA and DSP in recent years could offer a fundamental response to the real-time SAR machine problem of large-scale computing. In addition, the continuous creation of high-speed serial bus architectures, in particular the VPX and embedded interconnect buses such as SRIO, PCIE, could solve the conventional mutual parallel bus bottleneck, smash the data transfer slavery and promote the reconstruction, processor node extension. After decades of research, they have achieved a high resolution based on the imaging algorithms. The real-time radar signal processing platform has reached a comparatively mature level. Another problem will be how to co-optimize the SAR imaging algorithm and hardware device architecture to construct a high-performance, energy-efficient, universal radar signal processing framework.

The paper proposes a model for the scalable real-time signal processing method of high performances that is a modern approach by optimizing the use of established computing tools to work out the above issue. This paper's reminders are organized as follows. Section II analyses each of the SAR system's modules and its key functions. The hardware structure of the scalable high-speed real-time SAR signal processing module is introduced in Sectional. The programme design and experiment findings are then proposed in section IV. Section V requires a conclusion.

II. ABOUT SAR MACHINE BASED PRESENTATION

Our radar device consists of many sections, including the antenna, receiver, AD, DA, pre-processing portion, section of signal processing, compression part of JPEG image, module of monitor and console. It may also be separated modularly into control node, I/Module, net switching module, timing module and processing module.

Control module: It carries out both mission preparation and machine control.

The high-speed configurable SRIO, PCIE, Gibe net switching modules centered on the VPX structure, the transmission rate of which is up to 6,125 GB/s, could provide the data flow interconnection.

The central unit of the device is the signal processing module, which realizes SAR imagery algorithm mapping.

The IO module is responsible for interacting with external devices on the interface surface, including DAC, ADC, etc.

Timing module: A set of coordinated needs, such as the PRT, bowmen sampling, AD sampling and soon, could be accomplished through the purely synchronization timing network.

Fig.1 explains how these modules in our framework map to various boards.

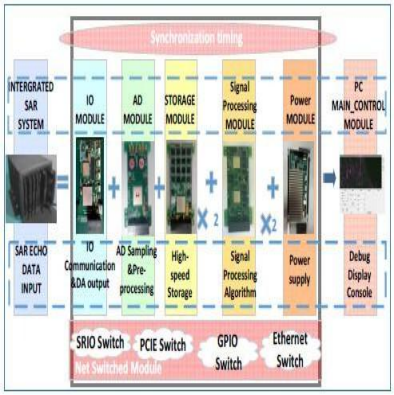

Fig. 1. SAR System Structure

III THE HARDWARE IMPLEMENTAION OF THE HIGHPERFORMANCEREAL-TIME SIGNAL PROCESSING SYSTEM

A. Hardware Platform of the Signal Processing Subsystem

The key considerations in the nature of the signal processing hardware platform are the strict restrictions on power usage and scale, high-speed data transmission and sophisticated computing of SAR imaging algorithms at the period. At the same time, the processing platform has been placed up to higher specifications with the tremendous rise of data volume and volumes of computation. We build ate layer PCB signal processing board based on the VPX 3U standard (100mm by 160mm) using the multi-coreTMS320C6678, thoroughly understanding the computation-intensive problems and other specifications. Its outstanding characteristics are shown as follows:

Processing performance: On the signal processing board, there are 2 bits of TI's DSPTMS320C6678 that are the board's central processing units. The TMS320C6678 Multicourse Fixed and Floating Point Digital Signal Processor are based on eight C66xCorePac DSPs built into TI's Keystonemulticore architecture. Each core performs up to 10 GHz at 1.0 to 2.5 GHz and the system will achieve a peak output of 320 GMACS or 160 GFLOPS [6].

Storage capacity: 32KB L1P, 32KB L1D, 512KB L2 per core and 4MB of eights core shared MSM are accessible. In addition, each DSP has 2GB of DDR3 memory.

Output of data exchange: The two DSPs are connected to each other by a 4Line 50Gbps Hyperlink high-speed bus that offers a fundamental connection for the expansion of the computing node. In addition, the key buses for the echo data input over the board are the high-speed SRIO (6.25Gbps), PCIE (5Gbps) of each DSP. The Gibe is accountable for the accuracy of the imaging data.

Other design: The single FPGA (XC3S200AN) on the board is primarily used for time management, power sequences and configuration of their parameters. Timing module, power module are also incorporated on it.

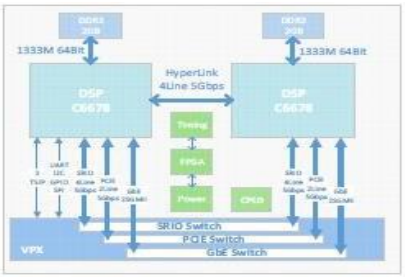

Fig. 2. Signal Processing Board Hardware Architecture

Fig. 3. Signal Processing Board

The computing-intensive issues may be solved with its efficient computation capacity and high-speed data transmission. At the same time, the high-performance hardware platform offers a fundamental assurance for the design and restoration of applications, extending the processing nodes to keep up with the constant developments of SAR imaging algorithms and changing specifications of different working modes.

B. Nodes of processing and Subsystem Processing Procedure

More processing and storage resources are required for high-resolution and wide-swath real-time imaging. Thus, two DSPs linked by the Hyperlink on one signal processing board could be merged into a virtual single node by the modification of software programming. Fig.4 shows the remodeling processing node.

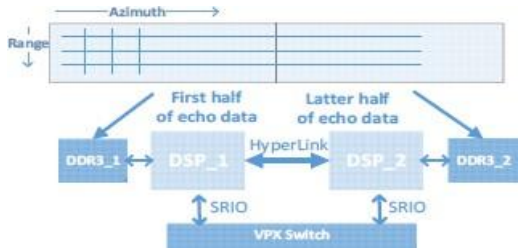

Fig. 4. The Diagram of a Virtual Processing Node

Every DSP has 2 G Byte DDR3 memories on the signal processing board. The storage capacity could be expanded to 4 GB by the rebuilding of the processing node, which ensures that picture mode could be run with 32 K * 16 K (4 GB) complex points. In Fig.4, the data in a data-processing granularity is similarly split into DDR3-1 and DDR3-2, where the data is continuous in a range section, and it is half of the full initial in the azimuth line.
There are 2 bits of computing board in our radar scheme, that is, two virtual processing nodes (Ping node and Pong node). To separately process the respective data frame, these two nodes perform the same central computing programme. Such nodes follow the concurrent computing approach of pipelines. Meanwhile, DSPs process a portion of the entire data frame in parallel within the processor node. The data flow for the processing of the device is seen in Fig.5. This structure thoroughly puts into action the matching efficiency of encoding, transmission and memory space.

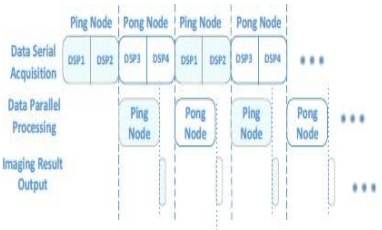

Fig. 5. Data Flow

IV. APPLICATION EXAMPLE

A. Real-time Imaging Algorithm

SAR is side-looking imaging radar of high-definition resolution. The SAR echo model can be seen from the point of view of signal processing as the convolution between the coefficient of backscattering of the separate targets on the ground σ ⁇ (x, r) and the $h_1(x,r)$, $h_2(x,r)$ [9].

$$s(x,r)=\sigma(x,r)\otimes h_1(x,r)\otimes h_2(x,r) \quad (1)$$

The impulse response spectrum is h (x, r), and the azimuth impulse response is 2h (x, r). Therefore, the process of SAR imaging is to recover the targets' backscattering coefficient. There are significant problems that need to be addressed about the real-time imaging algorithm. Second, in particular, the UAV (unmanned) airborne and space-borne platform.

Aerial Vehicle) device can be quickly impacted by the airstream or any poor flight climate, it would be very important to provide an outstanding picture algorithm output to cope with the worst flight state of the platform. At the same time, considering the minimal hardware resources and computational power, another challenge will be how to refine the well-designed algorithm as far as possible. Some mature algorithms are currently commonly used in time and frequency domain SAR imaging, such as BP and related enhanced algorithms, RD algorithms, CS algorithms, etc. Among them, the RD algorithm was selected to adopt the real-time imaging platform in accordance with the estimation of difficulty, stability and interface characters.

In real-time SAR imaging, the Range-Doppler (RD) algorithm [4] is the first developed and commonly used. The physical definition is visualized to approximate a 2D filter [5] from the spectrum and azimuth axis, and then separate the two-dimensional processing into one-dimensional processing by taking advantage of its reparability. The RCMC will be necessary for the point goal focusing effect, as in high-resolution situations. The RD algorithm primarily involves the calculation of the frequency rate of Doppler, Range compression, Range Cell Migration Correction (RCMC) and Azimuth compression. The detailed algorithm flow chart for the SAR imaging mode is shown as Figure 6.

Fig. 6. Imaging Algorithm

B. Evaluation

The execution period is critical in order to assess the signal processing module's efficiency. In particular, in the case of 8192, we evaluated the execution period of each stage of the RD algorithm alluded to earlier by 16384 complex point data with 1 piece of DSP. In Fig.7, the consequence is seen.

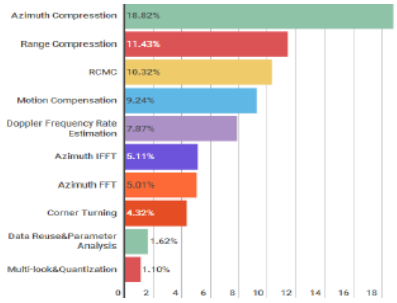

Fig. 7. Time Consumption of SAR Imaging Operation

We could easily see that the most computer-intensive measures were the Azimuth Compression component and the Range Compression part. On that basis, instead of all the computation time, we just choose these two measures to calculate the enhancement of the whole process acceleration of the algorithm. First of all, we add the Speedup Ratio and Efficiency [7] [10] that are commonly used to determine the acceleration state of our device in the parallel measurement. The Speedup Ratio tests algorithm parallelism by changing the execution time.

$$S(N)= T(1)/T(N) \qquad (2)$$

Where T (1) is the processing period performed by one processing device for all the activities with one data granularity. T (N) accounts for N parallel processing units' execution period. The Performance E (N) processor is specified based on the Speedup Ratio. It may help to evaluate the real parallel processing performance of each processor in the processing unit.

$$E(N)=S(N)/N \qquad (3)$$

N refers to the processor number in a processing unit. The result of accelerating Rate and Paralleling efficiency of the SAR processing with the image of 8192 by 16384 complex points is shown as Table I.

TABLE I. ACCELERATING TIME OF THE SAR PROCESSING WITH IMAGESIZE OF 8192 POINTS BY 16384 POINTS

Pieces of DSP	*1Piece Of DSP*	*2Pieces of DSP*	*Speedup Ratio*	*Efficiency*
Azimuth Compression	2.25s	1.20s	1.87	93.9%
Range Compression	1.36s	0.72s	1.89	94.6%
Total Time	11.94s	6.53s	1.83	91.2%

These two phases scale well with the sum of DSP, both over 1.8 for the speedup ratios. If we introduce a DSP calculating cell, the execution period could be almost half of the original time and the parallel productivity equivalent to the division of the parallel cell's accelerating rate is almost 95 percent. The acceleration rate may not be the same as the amount of parallel cells, because of the effects of IO propagation and synchronization waste.

C. Signal Processing Subsystem Operating Mode and Performance

The radar is designed for multi-mode, such as the informative strip mode or investigation strip mode (3m*3m, 1m*1m, 0.5m*0.5m, 0.3m*0.3m 0.2m*0.2m resolution) and the spotlight mode (0.2m*0.2m resolution), according to project specifications. Except that the picture with 0.2mresolution is the single polarization image, both modes are the SAR multichannel fusion image. Otherwise, in the experiment experiments, the GMTI monitoring and searching modes were also configured and have excellent efficiency. They will not be present in scope, restricted to the duration of the post. The following photos are the detailed strip mode fusion image with 0.3m*0.3m resolution and the single-polarization image with 32K*16K (4GB) complex points with a large-scale 0.2m*0.2m resolution spotlight mode.

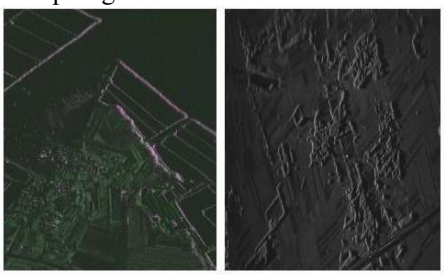

*Fig. 8.0.3m*0.3m polarization*

Mode fusion image&0.2m*0.2m single polarization image Please notice that while there are many modes of very low resolution, their imaging area is wider in order to take advantage of the calculating tools on the signal processing module, specifically, the lower resolution mode will have a wider imaging area. In general, each SAR mode's calculating burden is roughly equivalent. In order to explain their time consumption condition, we then select multiple real-time signal processing device operating modes.

TABLE II. EXECUTION TIME FOR KEY STEPS OF THE SAR PROCESSOR

Working Mode	*3m SAR*	*1m SAR*	*0.5m SAR*	*0.3m SAR*	*0.2m SAR*
Range Compression	2.74s	2.60s	2.61s	2.72s	2.74s
Corner Turning	5.18s	4.92s	4.93s	5.15s	5.18s
Frequency Rate Estimation	3.77s	3.58s	3.60s	3.75s	3.77s
RMCM	2.48s	2.35s	2.35s	2.46s	2.47s
Azimuth Compression	4.51s	4.29s	4.30s	4.48s	4.51s
Range Compensation	2.22s	2.10s	2.11s	2.20s	2.22s
Total	21.56s	20.47s	20.55s	21.42s	21.55s

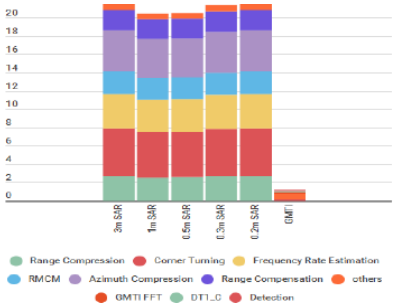

Fig. 9. ComparationExcution Time Results of the Different Mode

We could easily work out that the SAR modes range from the multi-polarization strip, according to Fig.9 For the estimation, mode (16K*16K*2 polarization channels=4GB) to single polarization Spotlight mode (16K*32K=4GB) will take approximately 22s. As for the GMTI detection mode, forming a picture with 2046*256 points needs just 1.47s. The efficiency of the signal processing module is sufficiently demonstrated by the above described active application cases.

V. CONCLUSION AGAINST

Summarizing all the introductions, including the effects of our signal processing system's hardware, software architecture and implemented instances, we may infer that the well-optimized system could fulfill the requirements of real-time high-performance SAR imaging and have the excellent computational capacity, reconfigurable hardware structure. It will not be restricted to a single form or class of algorithms because of the positive qualities of our method and genuinely achieves versatility for several SAR implementation scenarios.

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