Smart link designs I,II,III for communication in reconfigurable routers for network on Chip

Dr.Himani Mittal and Dr.Yogendera Kumar
School of Electrical, Electronics and Communication Engineering
Galgotias University, Plot no. 2, Sector 17-A, Yamuna Expressway,
Greater Noida, 201 301 (UP) India

Abstract—

In N.O.C links or various interconnections power dissipation contribute to major fraction. In fact, as technology shrinks, the power contribute of NoC links starts to compete with that of NoC routers. In this paper, we design link I , II , III with the help of MUX gating and various encoding techniques to reduce both power dissipation and energy consumption of NoC links .In this work ,we try to reduce power consumption in NoC links in three ways : Mux gating ,coding and encoding techniques .

This paper analyzes the behavior of Link design I,II,III in the highly structured environment of a network-on-chip (NoC).. After simulations , we obtain a reduction in total power dissipation and number of bit transitions up to 35% and 40%, respectively, without any significant degradation in terms of both performance and silicon area.

Keywords—Network on Chip (NoC);MUX gating; Encoding Techniques; Performance Analysis ; Power; Bit transitions.

I. INTRODUCTION

An NoC is an embodiment of a layered design approach [3]. This methodology considers on-chip communication and its abstraction as a micro-network consisting of particular layers, i.e. physical, data link, network, transport and application, each one having its own functions. Physical layer design should find a compromise between competing quality metrics and provide a clean and complete abstraction of the channel characteristics to the other layers. The data-link layer abstracts the physical layer as an unreliable digital link, where the probability of bit upsets is non-zero and increasing as technology scales down. Furthermore, reliability can be traded off against energy [5].

In this work we have done simulation analysis and performance evaluation of newly designed link design I , II , III. on chip design.

We would use the tool, Model Sim which has been extensively used in the research for design and evaluation of public domain computer network, to evaluate various design options for NOC architecture, including the design of links. In the following, we give a brief overview of our NOC links. In section I, we describe about various aspects of NOC links .Section II presents the literatutre survey.Section III gives brief explanation of Link Design I , II , III . Section IV gives a description for our simulation experiment, and in section V some experimental results and corresponding analyses are presented. Section VI gives comparision results Finally, we draw some conclusions in section VII.

II. LITERATURE REVIEW

Network-On-Chips (NoCs) links have been evolved considerably in term of power consumption ,performances, reliability and integration capacity. It is suitable for Dynamically Reconfigurable Multiprocessor on Chip systems as presented in [1]. [9] investigates an embedded transition inversion (ETI) coding that uses phase difference between the clock and data in the transmitted serial data to solve the problem of extra indication bit .For reducing bit transitions [7] investigates the data compression technique using Hamming Encoder and Decoder and] to reduce the test time with small area overhead on chip. The novel methodology also reduces the switching activity between the modified test inputs which lead us to reduce the test power dissipation during testing. Two different techniques are discussed [8] to reduce power consumption due to switching transition and cross talk. Technique on rearrange the data so that switching transition is brought down while the second technique, assures that power consumption due to cross coupling activity is reduced. This paper [10] discusses that in network on the major source of power dissipation is the network on chip links. If compared the power ratio between the network on chip links and router links are more power hungry than router.

III. LINK DESIGN I , II , III .

In the proposed Link Design I , II , III,we try to reduce power consumption in NoC links, in three ways : Mux gating ,coding and encoding techniques .

1. In Link Design I , with the use of MUX[2] gating path is reduced from source to destination by introducing diagonal path and the data once received is disconnected from the previous source.
2. In Link Design II , we reduce no. of transitions with the help of encoder and decoder . The encoder[4] will encode the data before placed onto data bus in such a way so that number of transition will reduce hence it will save switching power dissipation depending on the number of switching reduction. And other side decoder will decode the data into original form. These encoder and decoder can be used for off chip data transfer also.

3. In Link Design III ,with the help of multi coding technique we try to reduce transition activity in logic circuits .

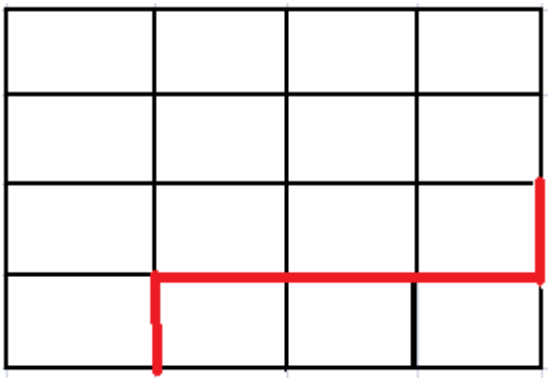

Fig. 1. Link Design I with path 5X.

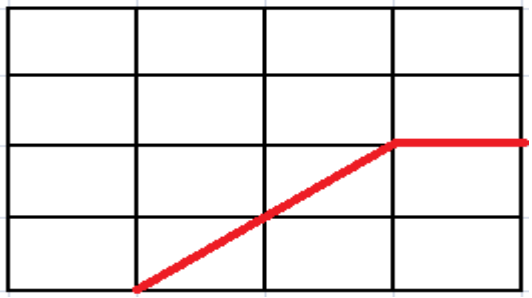

Fig.2. Link Design I with path 3X.

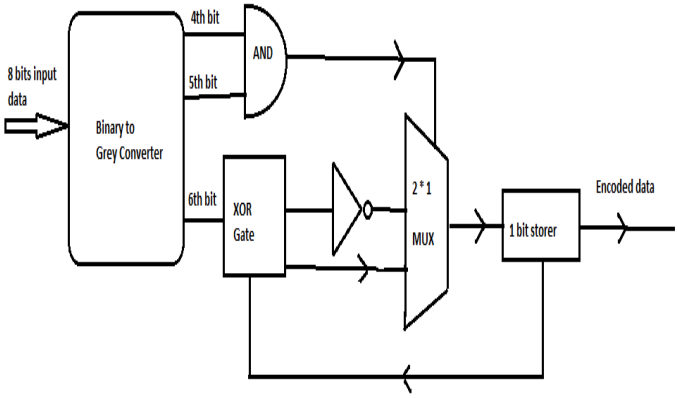

Fig. 3. Encoder of link design II.

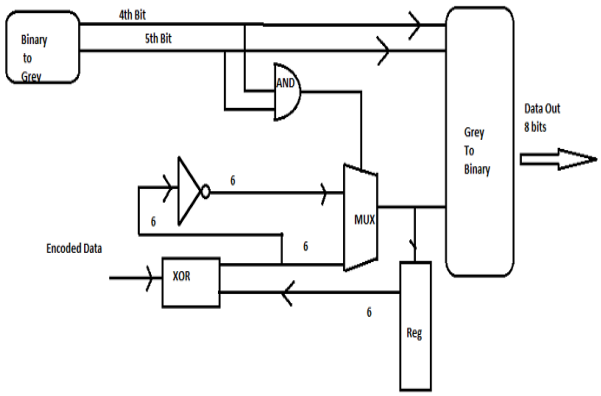

Fig.4. Decoder of Link Design II.

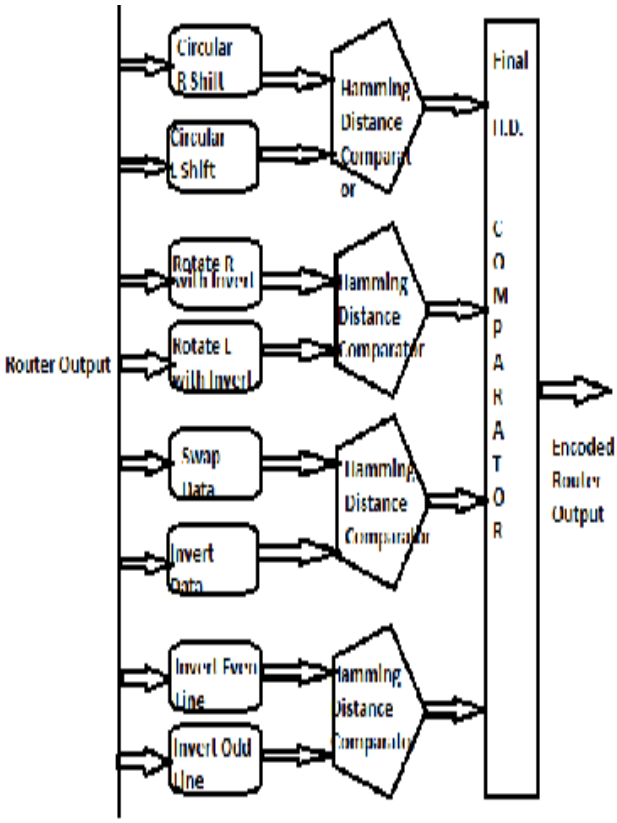

Fig. 5.Encoder of Link Design III.

IV. SIMULATION RESULTS :

Simulation refers to the verification of a design, its function and performance. It is process of applying stimuli to a model over time and producing corresponding responses from a model. Figures below show the simulation result of reconfiguration-al router. This simulation is performed on Model Sim PE Student Edition 10.4a.

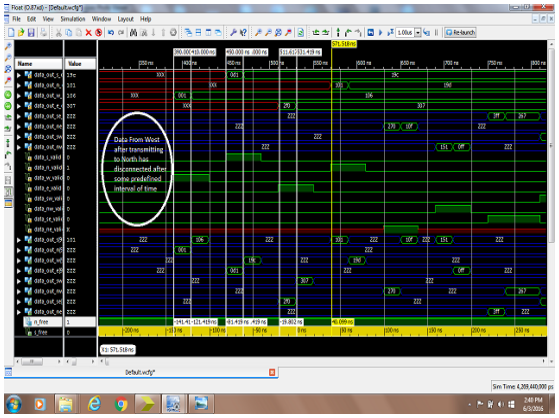

Fig.6a. Simulation of Link Design I

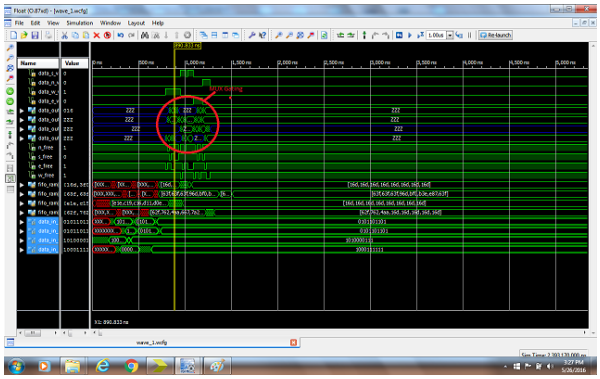

Fig. 6b. Simulation of MUX gating

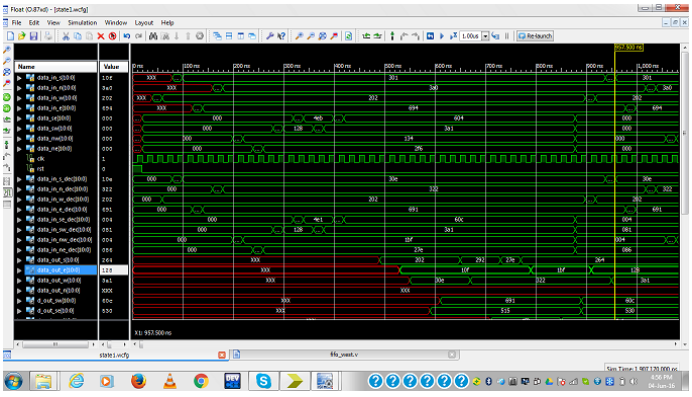

Fig.7 Simulation of Link Design II .

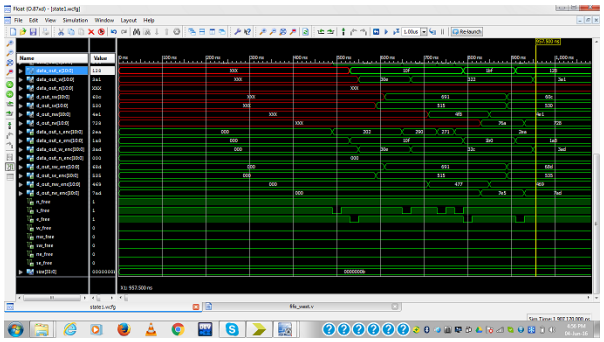

Fig.8 Simulation of Link Design III.

V. POWER AND AREA ANALYSIS :

Xilinx Power Analyzer (XPA) is a design tool used to analyze real design data. It is used to calculate power after design implemented in Xilinx ISE software. It uses the NCD file output from Place & Route (PAR) step.
Area analysis is also done by Xilinx tool Modelsim.It is done by synthesising routers and then seeing its synthesis report.

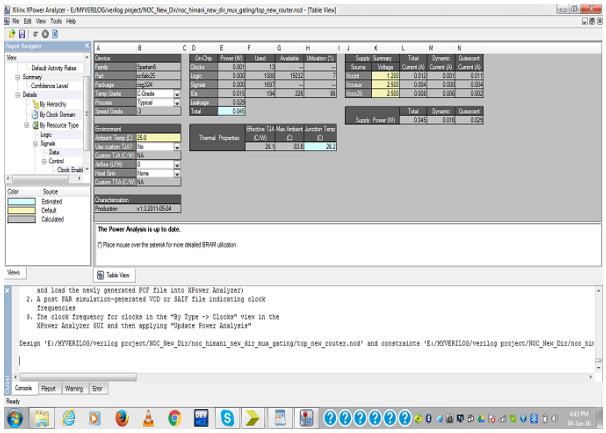

Fig. 10 Total Power Dissipation in Link Design I.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	574	30064	1%
Number of Slice LUTs	1347	15032	8%
Number of fully used LUT-FF pairs	393	1528	25%
Number of bonded IOBs	170	226	75%
Number of BUFG/BUFGCTRLs	1	16	6%

Fig.11 Design Summary of Link Design I.

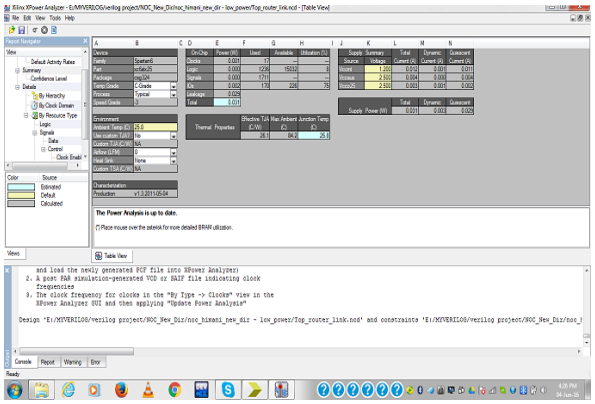

Fig. 12 Total Power Dissipation in ink Design II.

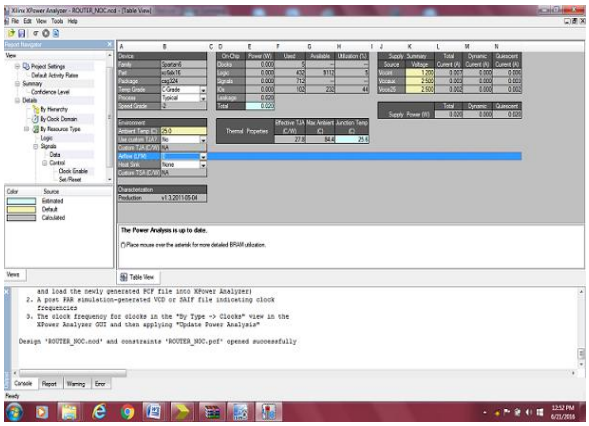

Fig. 13 Total Power Dissipation in Link Design III.

VI. COMPARISION OF FOUR ROUTERS :

Name of Technique	Power Consumtion(W)	Area Overhead (micrometer square)	Extra bus line needed
Link without technique	0.045	2016	No
link Design 1	0.034	1921	No
link Design 2	0.031	2175	No
link Design 3	0.02	1480	No

Fig.18 Performance Comparision of Four Routers.

(a) Power Comparision

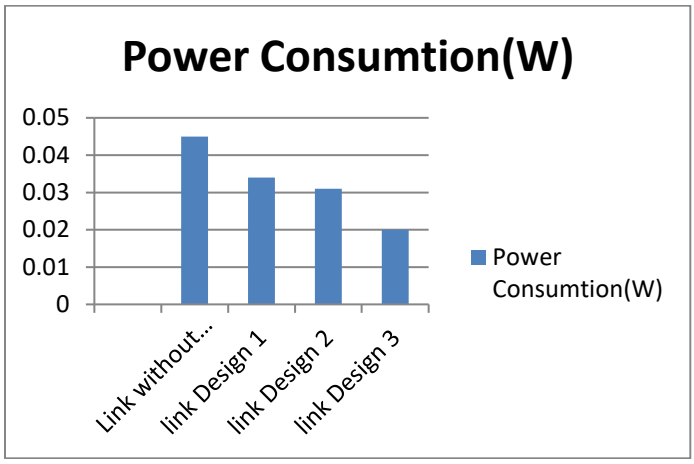

Fig.19 Comparision of power consumption of link designI,II,III.

(b) Area Comparision

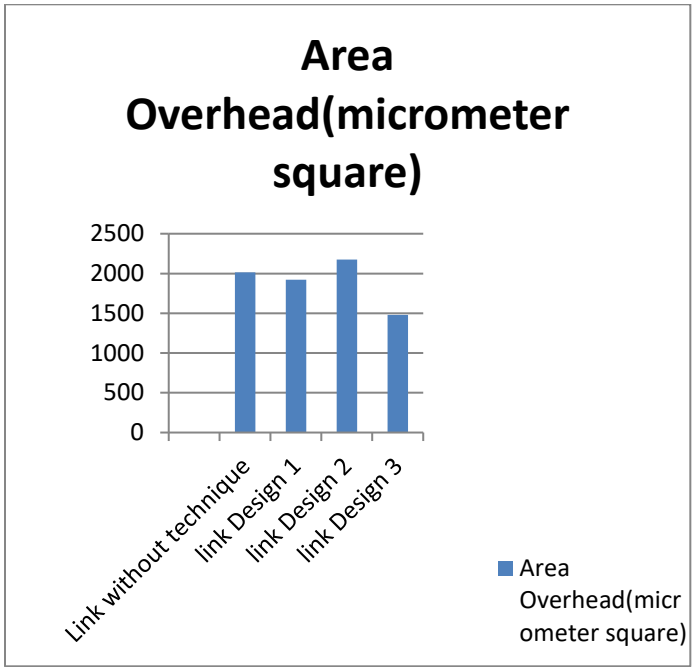

Fig.21 Comparision of area of link designI,II,III.

VII. CONCLUSION

Analyzing the results we find that average no. of bit transitions are reduced to more than 35% as we move from link design I to link design II .Simulations demonstrate a reduction of up to 55% in the number of bit transitions and up to40% savings in power consumed on the link

REFERENCES:

1. **[1** J.-S. Shen and P.-A. Hsiung , J. Shen and P. Hsiung , **"Dynamic Reconfigurable Network-on-ChipDesign"**: Innovations for Computational Processing and Communication , 2010 :IGI Global

[2]..M. Palesi, G. Ascia, F. Fazzino, and V. Catania, "**Data encoding schemes in networks on chip,**" IEEE Trans. Comput.-Aided Design Integr. Circuits Syst. , vol. 30, no. 5, pp. 774–786, May 2011.

[3].P. Sotririadis and A. Chandrakasan "**Low Power Coding Techniques Considering Inter wire capacitances**" In Proc. Of IEEE Conference on Custom Integrated Circuits (CICC'00), pp 507-510,2000.

[4].M.R.Stan and W.P.Burleson,"**Bus Invert Coding for Low power I/O"IEEE Trans VLSI Systems**,pp 49-58,March 1995.

[5]. N.K.Samala,R.Damu and B.Izadi "**Novel Deep Sub Micron Bus Coding for Low Energy**", In Proc of the International Conferences on Embedded System and Applications,pp 25-30,June 2004.

[6]. M.Madhu,V.S.Murthy and V.Kamakoti"**Dynamic Coding Technique for Low Power Data Bus**" Proceedings of IEEE Computer Society Annual Symposium on VLSI,pp 87-88 June 2003.

[7] . K. P. Sridhar, R. Agalya, D. Narmatha, B. Vignesh and S. Saravanan, "**Test data compression using Hamming Encoder and Decoder for system on chip (SOC) testing**," Circuit, Power and Computing Technologies (ICCPCT), 2014

[8]. D. N. Sarma, G. Lakshminarayanan and K. V. R. S. Chavali, "**A Novel Encoding Scheme for Low Power in Network on Chip Links,**" 2012 25th International Conference on VLSI Design, Hyderabad,2012,pp.257-261.doi: 10.1109/VLSID.2012.80

[9].C. T. Chiu, W. C. Huang, C. H. Lin, W. C. Lai and Y. F. Tsao, "**Embedded Transition Inversion Coding With Low Switching Activity for Serial Links**," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 21, no. 10, pp. 1797-1810, Oct. 2013.

[10]. Chetan S. Behere, Somulu Gugulothu, "**Power reduction in network on chip links"**, Green Computing Communication and Electrical Engineering (ICGCCEE) 2014 International Conference on, pp. 1-4, 2014.